CASES 2020

Call for Papers

International Conference on
Compilers, Architectures, and Synthesis for Embedded Systems
September 20-25, 2020, Virtual Conference

CASES is a premier forum where researchers, developers and practitioners exchange information on the latest advances in compilers and architectures for high-performance, low-power, and domain-specific embedded systems. The conference has a long tradition of showcasing leading edge research in embedded architectures for processor, memory, interconnect, and storage, as well as related compiler techniques targeting performance, power, security, reliability, predictability issues for both traditional and emerging application domains. We also invite innovative papers addressing design, synthesis & optimization challenges in heterogeneous, accelerator-rich architectures.

Journal-Track Submissions
Abstract: April 3, 2020
Full Paper: ~~April 10, 2020~~
April 17, 2020 (extended, firm)
Work-in-Progress Submissions
~~June 5, 2020~~
June 12, 2020 (extended)
Notification of Acceptance
July 6, 2020 (both tracks)

Compilers for Embedded Systems: Compilation for power and performance; Compiler support for CPU, GPU, reconfigurable computing, heterogeneous and domain-specific multi-core SoC; Compilation for memory, storage, and on-chip communications.

Processor Architectures: Embedded and mobile processor micro-architecture, Multi- and many-core processors, GPU architectures, Reconfigurable computing including FPGAs and CGRAs, Application-Specific processor design, 3D-stacked architectures; Power- and energy-efficient architectures.

Memory and Storage: Memory system architecture; Non-volatile and other emerging memory technologies; Scratchpad memory, caches and compiler-controlled memories; storage organization including flash storage.

On-chip communication and I/O: Networks-on-chip architectures and design methodologies; on-chip communication synthesis, analysis, and optimization; I/O management in embedded systems.

Accelerators: Synthesis, optimization, and design-space exploration of high-performance, low-power accelerators; Novel design paradigms and compilers for accelerators including approximate computing, machine learning and big-data analytics.

Security, Reliability, and Predictability: Secure architectures, hardware security, and compilation for software security; Architecture and compiler techniques for reliability and aging; Modeling, design, analysis, and optimization for timing and predictability; Validation, verification, testing & debugging of embedded software.

Emerging Applications: Architectures, accelerators, and compilers for machine learning, neuromorphic & cognitive computing, data analytics; biologically inspired computing systems.

Trustworthy IoT: A special day will be jointly organized by the conferences in ESWEEK. Articles aligned to the topics of interest for CASES, with distinct focus on Trustworthy IoT are most welcome.

CASES 2020 has a dual publication model with two tracks: Journal track papers will be published in the IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD) and Work-in-Progress track papers will be published in the ESWEEK Proceedings. More details at http://www.esweek.org/author-information

ESWeek General Chairs:

Tulika Mitra, National University of Singapore, SG
Andreas Gerstlauer, University of Texas at Austin, USA

CASES Program Chairs

Partha Pratim Pande, Washington State Univ. USA
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